A 90 nm Communication Technology Featuring SiGe HBT Transistors, RF CMOS, Precision R-L-C RF Elements and 1 um^2 6-T SRAM Cell

K. Kuhn, M. Agostinelli[#], S. Ahmed, S. Chambers, S. Cea*, S. Christensen[1], P. Fischer, J. Gong*, C. Kardas, T. Letson, L. Henning[1], A. Murthy, H. Muthali, B. Obradovic*, P. Packan*, S. W. Pae[#], I. Post, S. Putna, K. Raol, A. Roskowski, R. Soman, T. Thomas, P. Vandervoorn, M. Weiss and I. Young

Portland Technology Development, * TCAD, [#] QRE, [1]ICG, Intel Corporation, Hillsboro, OR 97124, USA.

Abstract

This paper presents a highly-manufacturable process technology featuring SiGe HBT devices fully integrated into a 90 nm leading-edge high performance CMOS technology. The technology was developed on a 300 mm wafer platform, and supports process elements including RF CMOS devices, a MIM capacitor, precision resistors, high-Q inductors and varactors.

Introduction

Product designs incorporating both CMOS and BJT active elements have emerged as a potential growth technology for the communications marketplace. Unlike historic designs, these new products are utilizing approaches where digital cells from well-characterized libraries are being mixed with specialized analog and RF modules. This permits the designer to leverage the manufacturing and performance advantages of high-performance digital CMOS while retaining specialized analog circuit functionality.

Base Technology Features

This paper describes a 90nm feature-rich process technology optimized for products in the communication marketplace. The technology is derived by integrating a variety of active and passive elements into the base 90nm high performance digital CMOS technology introduced in [1]. The base technology supports a 1.0 μm^2 6-T SRAM and offers a 7-layer Cu metal back-end with low-k dielectric. 193 nm lithography is used to pattern the poly-silicon gate layer permitting a 1.0 μm^2 6-T SRAM cell without the use of a local interconnect layer. The interconnect technology uses dual damascene copper to reduce the resistances of the 7 layers of interconnects. Carbon doped oxide (CDO) is used as inter-level dielectric (ILD) to reduce the dielectric constant.

Additions to the base technology to support the communications features include low power and high voltage CMOS devices, performance and high voltage SiGe HBT BJT devices, a MIM capacitor, a metal thin film resistor, unsilicided poly resistors as well as inductor and varactor elements.

CMOS

The need to improve performance and density while minimizing active and passive power is a well-known challenge for CMOS scaling. The requirements of the communications marketplace are even more rigorous due to the larger operating temperature range and the necessity to reduce cost. To address these requirements, this technology offers process options and standard cell libraries to permit designers to selectively target either performance or low power operation. More specifically, the process offers a performance option which includes the high and low V_T devices described in [1] as well as high and low V_T devices with 50Å (physical) gate oxide thickness. A 1.8V analog device with 50Å (physical) gate oxide thickness is also supported. The low power option replaces the high and low V_T devices with a nominal V_T device with 15Å (physical) gate oxide thickness. Performance and low power standard cell libraries are offered in 80 and 90 nm (drawn) and can be used interchangeably between the performance and low power options. Table I summarizes the matrix of specifications for the CMOS devices including the low power devices (short and long gate), the analog devices (nominal V_T) and the I/O devices (high and low V_T).

SiGe Bipolar Junction Transistor

BJT devices offer noise and transconductance advantages over CMOS in mixed signal applications [2]. Therefore, this process offers performance and high voltage versions of a quasi-self-aligned (QSA) NPN SiGe HBT device. World-class optical lithography and ultra-narrow base profiles of SiGe:C are leveraged to maximize the performance of the QSA geometry.

		Low Power		Analog		I/O	
Parameter	units	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
Vcc	Volts	1.2	1.2	1.8	1.8	2.5	2.5
Drawn Lgate	μm	0.080 / 0.090	0.080 / 0.090	0.26	0.26	0.32/0.36	0.32/0.36
Physical gate oxide thickness	Å	15	15	50	50	50	50
Threshold voltage (high/low)	mV			378	338	465 / 240	390 / 230
Threshold voltage (short/long)	mV	420 / 420	400 / 400				
Idsat (high/low)	mA/μm			0.47	0.25	0.58 / 0.648	0.28 / 0.32
Idsat (short/long)	mA/μm	1.0 / 0.9	0.5 / 0.4				
Ioff @ nominal (high/low)	nA/μm			2.45	0.6	2.8E-2 / 3	1.2E-2 / 1.6
Ioff @ nominal (short/long)	nA/μm	15 / 3	6 / 1				
gm (high/low)	mS			0.45	0.22	0.342 / 0.337	0.122 / 0.11
gm (short/long)	mS	2.6 / 2.4	0.9 / 0.7				
Gds (high/low)	mS			0.44	0.26	0.19 / 0.197	0.114 / 0.2
Gds (short/long)	mS	2.0 / 1.5	1.4 / 0.9				

TABLE I – CMOS DEVICE SPECIFICATIONS

NPN SiGe HBT

The baseline SiGe HBT is a 0.21 x 7.0 μm^2 QSA BJT device. Carbon doping is used in the base to suppress B diffusion and provide a wider process margin without impacting DC performance [3,4]. The baseline device has f_t = 130 GHz and f_{max} = 100 GHz at V_{bc} = 1 volt (V_{ce} = 2 volts). Fig. 1 presents H_{21} and Mason's gain data and Fig. 2 presents I_C versus frequency data for f_t and f_{max}. Higher f_t can be obtained on the baseline geometry by trading off *fmax* for f_t. Fig. 3, presents f_t = 150 Ghz at with f_{max} = 85 GHz for V_{bc} = 1 volt (V_{ce} = 2 volts). Cross-wafer and wafer-to-wafer process stability is illustrated by Fig. 5, which presents fully automated RF test data for a typical baseline lot running on 300mm wafers (within wafer 1-σ = 4.2GHz, wafer-to-wafer 1-σ = 3.1GHz).

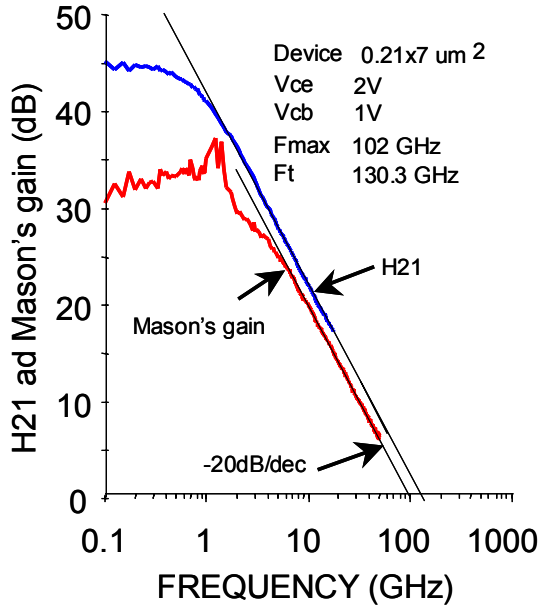

Figure 1: H_{21} and Mason's gain data versus frequency for the 0.21 x 7.0 μm^2 performance device at V_{bc} = 1 volt, V_{ce} = 2 volts.

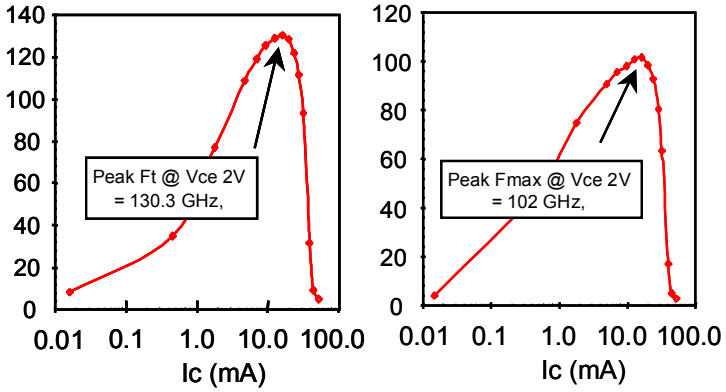

Figure 2: f_t and f_{max} as a function of I_C for the 0.21 x 7.0 μm^2 baseline device.

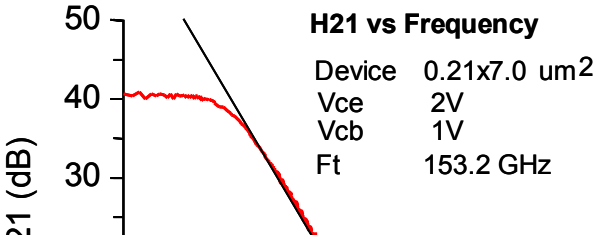

Figure 3: H_{21} versus frequency for the 0.21 x 7.0 μm^2 baseline device optimized by trading off *fmax* for f_t.

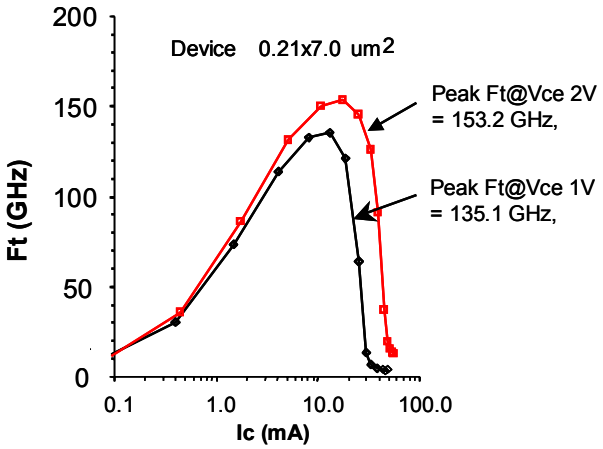

Figure 4: f_t as a function of I_C for the 0.21 x 7.0 μm^2 f_t–optimized device for several V_{bc} and V_{ce} values.

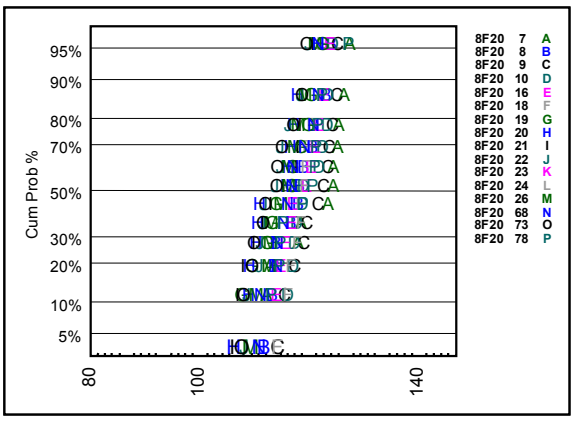

Figure 5: Automated test data for the baseline device showing within wafer and wafer-to-wafer variation on 300 mm wafers.

Passive elements

A key difference between digital and mixed-signal processes is the presence of accurate passive elements. In the digital design world, performance is largely determined by active elements. In contrast, in analog/mixed-signal design, performance is usually limited by the accuracy of the passive components [5].

Inductors

The basic inductor element is fabricated in MT7 with an MT6 underpass. Small-valued, precise, high-Q inductors are employed in circuits such as RF transceivers. Larger, lower-Q devices are used for impedance matching and gain control. A library of basic and high-Q inductors has been implemented to meet the needs of communication products (the high-Q library inductors are summarized in Fig. 6).

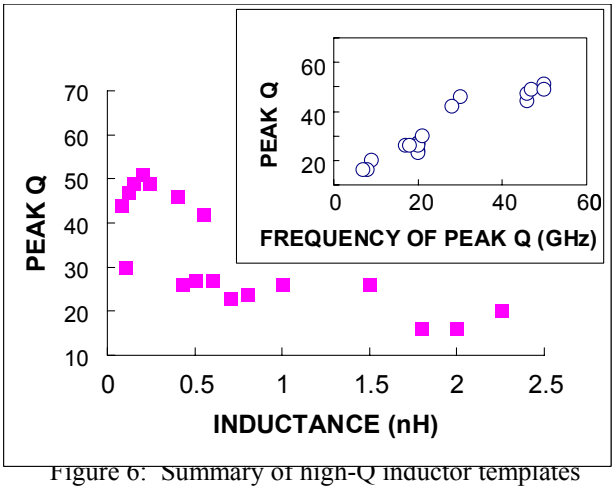

Figure 6: Summary of high-Q inductor templates

A very difficult factor in inductor process design is minimization of the impact of parasitic elements. High resistivity substrates and parasitic control of local design environments (with templates) can significantly improve Q (Fig. 7).

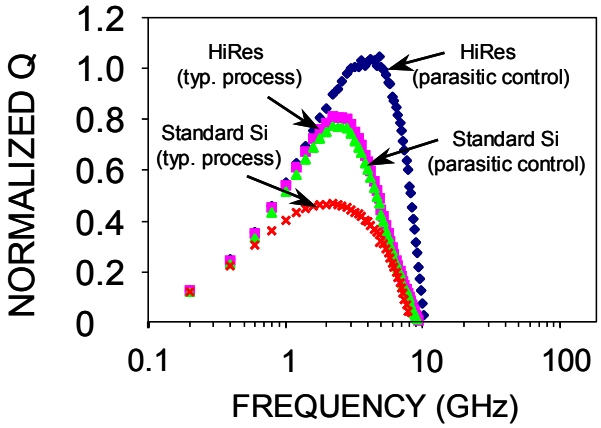

Figure 7: Improvement in inductor Q resulting from high resistivity substrates (HiRES) and control of local design environment with templates (parasitic control).

MIM capacitors (and resistors)

Metal-insulator-metal (MIM) capacitors are supported as a precision capacitive element. The basic MIM element is fabricated between MT6 and MT7. A PECVD-deposited thick SiN film is used as the insulator. Ta connected to M7 Cu layer is used as the upper electrode while M6 Cu is used as the lower electrode. (Precision metal resistors are fabricated opportunistically using the Ta layer.) MIM precision capacitors can be manufactured accurately (Fig. 8 shows manufacturing data) and reliably (Fig. 9) and possess excellent linearity with temperature and voltage (Fig. 10).

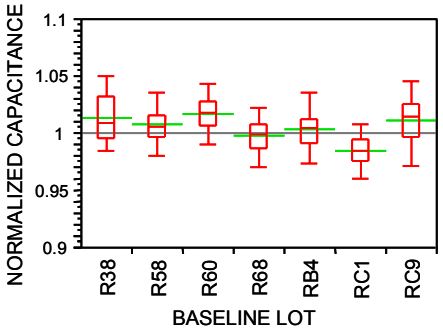

Figure 8: Baseline process data illustrating within lot and lot-to-lot stability on 300 mm wafers.

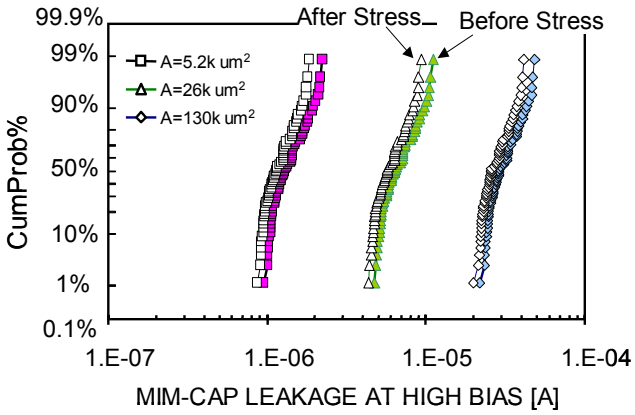

Figure 9: Leakage data before and after short stress (at very high voltage) illustrates no MIM capacitor defect issues.

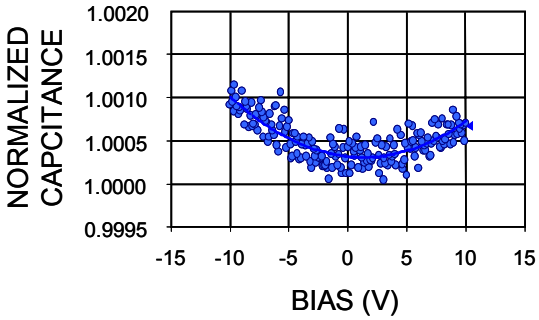

Figure 10: Normalized MIM capacitance illustrates the excellent linearity of the MIM capacitor.

RF CMOS

CMOS devices possess linearity advantages over BJTs and find application in RF and mixed signal circuits where noise is not a constraint. Device geometry is very critical for CMOS evaluation, and a folded geometry similar to that reported in [6] was used for characterization. Device performance on a 6-fingered $Z = 2.5\mu m$, $L = 0.08\mu m$ structure is ft = 150 GHz and $fmax$ = 80 GHz at V_{ds} = 1.2V and V_g = 0.8V). Figure 11 presents H_{21} and Mason's gain data.

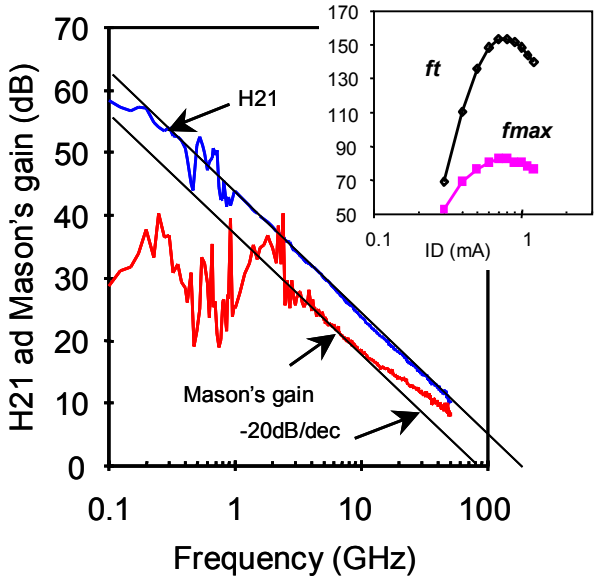

Figure 11: H_{21} and Mason's gain data versus frequency, as well as ft and $fmax$ versus I_D, for a 6-fingered device with $Z = 2.5\mu m$, $L = 0.08\mu m$ at V_{ds} = 1.2 volt, V_g = 0.8 volts.

Reliability

Communications technologies pose special challenges for reliability validation due to the multiplicity of features. The following reliability elements have been demonstrated:

Gate oxides: The 15Å and 50Å gate oxide devices have target voltages of 1.2 and 2.75 volts respectively. Reliability validation shows they are capable of supporting a Vmax of 1.5V (for the 15Å) and 3.8V (for the 50Å) at 125C. (The 12Å device is discussed in [1].)

MIM capacitors: Small area MIM capacitors have been evaluated for bias-temperature instability and have been found to be stable to within +/- 0.2% through specified product lifetimes at low frequency. Voltage and temperature acceleration of time-to-breakdown (TDDB) studies on the MIM capacitors indicate acceleration parameters similar to published results. Short stress at very high voltage shows no extrinsic MIM CAP defect leakage tails (Fig. 6).

Inductors: Stress studies of low frequency inductance show stable inductance +/-0.1% over extreme stress conditions (close to 100mA compliance stress).

BJT: Using an industry-typical failure criteria of 10% degradation in β, a lifetime of greater than 20 years was obtained at a constant reverse bias voltage of approximately –2.1V. For acceptable β degradation during forward active device operation, a maximum J_C of 1mA/μm has been computed. Extensive stressing using both reverse emitter-base stress and forward active stress has not revealed any significant f_t or f_{max} degradation.

Early learning vehicles

To provide good yield and reliability coverage for the feature-rich communications design environment, development design validation vehicles are being fabricated which contain test circuits and product look-aheads to support process development and early design validation (see Figure 12).

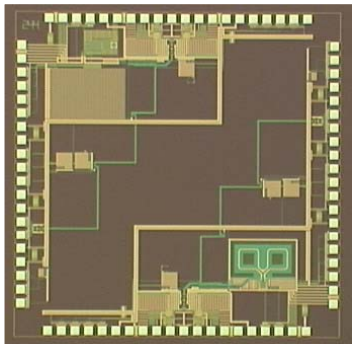

Figure 12: Photomicrograph of a functional test circuit typically used on 10 Gb/s SerDes products.

Conclusions

A feature-rich 90 nm communication process has been developed. This technology shares high performance digital CMOS features with the 90 nm logic technology described in [1] and adds specialized analog device elements and SiGe HBT transistors.

Acknowledgements

The authors wish to acknowledge the significant contributions of M. Bohr, C. Simonsen and S. Thompson (PTD), F. Buckley, I. Chao, S. Dreyer, U. Keil, G. Prat and M. Vinter (ICG), Richard Basco (PTD), Kevin Redmond (STTD), Weikai Shih (TCAD), Bruce Woolery, Scott Hareland and Shing Lau (TD Q&R).

References

[1] S. Thompson, et al. to be presented IEDM, December 2002.
[2] D. Harame, et al. IEEE BTCM 2.1, pp. 36-43.
[3] H.J. Osten, et al. IEDM 97-803, pp. 32.4.1-32.4.4
[4] H. Rucker, et al. IEDM 99-345, pp. 14.4.1-14.4.4
[5] R. K. Ulrich, et al. *IEEE Circuits and Devices*, Sept. 2000, pp. 17-25.
[6] L. F. Tiemeijer, et. al. *IEDM Technical Digest International*, 2001, pp. 10.4.1-10.4.4.